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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/877,033	06/11/2001	Shinji Fukasawa	108075-00062	9808

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EXAMINER	
DIMYAN, MAGID Y	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/877,033	FUKASAWA, SHINJI	
	Examiner	Art Unit	
	Magid Y Dimyan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action pertains to Application No. 09/877,033, filed 11 June 2001. Claims 1 – 20 remain pending in this Application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,490,715 to Moriwaki et al. (hereinafter, "Moriwaki") in view of U.S. Patent No. 5,680,064 to Masaki et al. (hereinafter, "Masaki").

4. Referring to claim 1, Moriwaki discloses a semiconductor device including a first power supply line that corresponds to a first power supply voltage and a second power supply line that corresponds to a second supply voltage, wherein the first power supply voltage differs from the second supply voltage (see Figs. 5A, 5B, 6; col. 8, lines 34 – 56). Furthermore, Moriwaki teaches: the inclusion of at least one function block (Fig. 2, block 121); the use of standard cells (col. 2,

lines 31 – 53); and a level converter cell (Figs. 5A and 5B). But Moriwaki does not disclose the elements of: (a) a first standard cell arranged in the function block having a first power supply terminal connected to a first power supply line; (b) a second standard cell having a second power supply terminal connected to the second power supply line; and (c) a level converter cell aligned with the first and second standard cells and having a third power supply terminal connected to a first power supply line and a fourth power supply terminal connected to the second supply line. However, Masaki teaches level converter methodologies for IC designs such as gate arrays (see Fig. 5; col. 10, lines 28 – 40) that in fact cite these additional elements as shown in Fig. 1. Block 1 in Fig. 1 is a function block having a first power supply terminal (VDD1) connected to a first power supply line (Fig. 5); block 2 is a function block with a second power supply (VDD2) terminal connected to a second supply line (Fig. 5); and block 3 is a level converter with a third power supply terminal connected to the first power supply line (VDD1) and a fourth power supply terminal connected to the second supply line (VDD2). Thus, Moriwaki and Masaki in combination teach all the elements of the claims. Since mix voltage designs are now very common in complex circuit designs such as Standard Cell, ASIC and SoC devices due to power dissipation and performance concerns, it would therefore be obvious to a person of ordinary skill in the art at the time of the invention to combine the teachings of both inventions to obtain the same claimed elements.

5. As for claims 2 and 3, see Masaki – Figs. 1 and 5, which show the first (linear) power supply line VDD1 connecting the first and third terminals, and the second (linear) power supply line VDD2 connecting the second and fourth terminals, as claimed.

6. As per claims 4 and 5, see Moriwaki - Fig. 6; col. 8, line 50 – col. 9, line 25 which cite the claimed elements pertaining to the level converter cell, and the standard cell outside the function block.

7. Referring to claims 6 and 7, see Moriwaki – Figs. 2, 5A, 5B and 6; col. 5, lines 22 – 33, which recite how the standard cells, function blocks and level converter cell are arranged, as claimed.

8. Referring to claim 8, Moriwaki teaches a semiconductor device comprising: (a) a plurality of blocks including a first block and second block (Fig. 2); (b) the use of standard cells (col. 2, lines 31 – 53); (c) a level converter cell (Figs. 5A and 5B). On the other hand, Masaki recites all the other claimed elements of: (a) a first standard cell arranged in the function block having a first power supply terminal connected to a first power supply line; (b) a second standard cell having a second power supply terminal connected to the second power supply line; and (c) a level converter cell aligned with the first and second standard cells and having a third power supply terminal connected to a first power supply line and a fourth power supply terminal connected to the second

supply line. The motivation for combining the two disclosures to obtain the same claimed invention is cited in (4) above.

9. As per claims 9 - 11, see Moriwaki – Fig. 6; Masaki Figs. 1, 5 and 22; which show in combination how the standard cells, function blocks and level converter cell are arranged, as claimed.

10. As per claims 12 - 15, see Moriwaki – Figs. 5A and 5B; and Masaki – Fig. 1; which show in combination how the first, second, third and fourth power supply terminals and linear supply lines are connected to the standard cells and to the converter cell, as claimed herein.

11. Referring to claim 16, Moriwaki and Masaki in combination teach a designing apparatus for generating layout data of a semiconductor device (Moriwaki – Fig. 1), wherein the semiconductor device is provided with a plurality of blocks including a first block and a second block (Moriwaki – Fig. 2), a plurality of first standard cells arranged in the first and second blocks, a second standard cell arranged between the first and second blocks (Moriwaki – Figs. 2, 5A, 5B; col. 8, lines 19 – 56), and a level converter cell (see also Masaki – Fig. 1); wherein each of the standard first standard cells have a first power supply terminal formed in the first region, the second standard cell has a second supply terminal formed in the second region, and a level converter cell has a third power supply terminal formed in the first region, and a fourth power supply terminal

formed in the second region (Moriwaki – Figs. 5A and 5B; Masaki – Figs. 1 and 22), the designing apparatus comprising: a processor, wherein the processor obtains a netlist data of the device (Moriwaki – Fig. 1; col. 5, lines 14 – 42), sets a power supply voltage of each block based on the netlist data, sets a voltage between the blocks based on the power supply voltage of each block, generates the level converter cell based on the voltage between the blocks, and arranges the level converter cell in one of locations in or between the blocks in accordance with the power supply voltage and the voltage between the blocks so as to align the level converter cell between the first and second standard cells. See (4) – (10) above, as well as Moriwaki – Fig. 1, 5A, 5B; and Masaki – Figs. 1 and 22, which teach all the claimed elements.

12. As per claims 17 and 18, see Moriwaki – Figs. 1, 6 and 7; col. 8, lines 34 – 56 which teach how the CAD system (designing apparatus) arranges the level converter cell, and aligns the level converter cell with the standard cells and with the blocks, as claimed.

13. Referring to claim 19, Moriwaki and Masaki teach in combination a computer readable storage medium storing a program for generating layout data of a semiconductor device having a plurality of blocks with a computer (Moriwaki – Fig. 1; col. 5, lines 14 – 33), wherein the semiconductor device is provided with blocks including a first and second block (Moriwaki – Fig. 2), a plurality of first standard cells arranged in first and second blocks, a standard cell arranged

between the blocks (Morikawi – Figs. 2, 5A, 5B, 6; and col. 8, line 19 to col. 9, line 10), and at least one level converter cell (Masaki – Figs. 1 and 22) between the standard cells and blocks, wherein each of the first standard cells have a first power supply terminal formed in the first region, the second standard cell has a second power supply terminal formed in the second region, and a level converter cell has a third power supply terminal formed in the first region, and a fourth power supply terminal formed in the second region (Masaki – Fig. 1), the program comprising the steps of: (a) obtaining netlist data (Moriwaki – Fig. 1, block 12); (b) setting a power supply voltage based on netlist data (Moriwaki – col. 5, line 33 to col. 6, line 27); (c) setting a voltage between the blocks based on supply voltage of each block (Moriwaki – Figs. 5A, 5B, 6 and 7); (d) generating the level converter cell based on the on the voltage between the blocks (see (c) as well as Masaki – Figs. 1 and 22); and (e) arranging the level converter cell in one of locations or in between the blocks so as to align the level converter cell with the standard cells (see Moriwaki – Figs. 5A and 5B; Masaki – Figs. 1 and 22). Thus, Moriwaki and Masaki cite all the elements of the claim.

14. Referring to claim 20, Moriwaki and Masaki in combination disclose a semiconductor device comprising: (a) a linear first power supply line for supplying a first power supply and a linear second power supply line extending parallel to the first power supply line for supplying a second supply voltage that is different from the first supply voltage (Masaki – Fig. 5); (b) a first block and a second block (Moriwaki – Fig. 2); (c) a plurality of first standard cells arranged in each of the

blocks having a predetermined shape and includes an end and a first power terminal connected to the first power supply line (Masaki – Figs. 1, 5 and 22; Moriwaki – Figs. 5A and 5B); (d) a second standard cell with substantially the same shape as the first standard cells and a second power supply terminal connected to a second power supply line (see above; Masaki – Figs. 1 and 5; Moriwaki – Figs. 5A and 5B); and (e) a level converter cell aligned with the first and second standard cells, wherein the level converter cell has substantially the same shape as the first and second standard cells (see above; Moriwaki – Figs. 5A and 5B) and includes an end, a third power supply terminal formed at a location separated from the end by the first distance and connected to the first power supply line, and a fourth power supply terminal formed on a location separated from the end by a second distance and connected to the second power supply line (see above; Masaki Figs. 1 and 22). Thus, Masaki and Moriwaki in combination teach all the claimed limitations.

15. The motivation for combining the teachings of Moriwaki and Masaki to achieve all the claimed elements of this invention is provided in (4) above.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pub. No. US 2002/0002700 to Inui et al. cites a method for designing a semiconductor device having a plurality of logic elements provided with a plurality of power supplies in which a power supply type name is given to each power supply in accordance with the purpose of the power supply in each logic element.

U.S. Patent No. 6,266,798 to Kanazawa et al. discloses a multi power supply IC evaluating method which is capable of detecting power supply voltage illegal connections, redundant connections, and potential redundant connections from connection descriptions contained in the multi power supply IC, and then automatically correcting each connection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Magid Y Dimyan
Examiner
Art Unit 2825

myd
1 October 2004

MYD

LEIGH M. GARBOWSKI
PRIMARY EXAMINER